Large-Scale Highly Aligned Nanowire Printing

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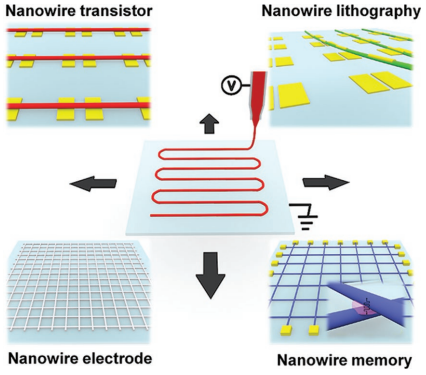
Nanowires (NWs) are 1D confined nanostructures; this geometry gives them unique properties that have been exploited in fabrication of high-density and high-tech electronic devices. Current method to produce NWs cannot fabricate large-scale-aligned NW arrays with precise control of length, orientation, location, and number of NWs individually; these inabilities hinder application of NWs in practical electronics. This paper describes e-nanowire printing, a method to print highly aligned NWs on a large scale, and then reviews recent progress in various electronic applications with highly aligned NWs. Finally, future research is suggested to advance nanoelectronics.



1. Introduction

Nanowire (NWs) have 1D confined nanostructure; as a result, they have unique electrical and physical properties, which have been exploited in various electronics applications including energy harvesting, chemical sensing, memory, logic circuits, optoelectronics, and bioelectronics.[1–20] Moreover, the high aspect ratio, high surface-to-volume ratio, mechanical flexibility, high-throughput, and inexpensive solution process to fabricate NWs are suitable for development of flexible, large-scale, and high-density electronic devices.

Electrospinning is a well-known process to fabricate various kinds of NWs; it allows mass production of very long and continuous NWs in easy, inexpensive, fast, and scalable ways.[21–39] Considerable research on NWs based on a broad range of materials from conductor to insulators and from organic to inorganic materials for electrospun NW-based electronics has been reported. However, electrospinning causes chaotic whipping of NWs during the fabrication, so they have randomly coiled structures.[21–31] As a result, they cannot fabricate high-density and uniform device arrays on a large-area substrate.

To improve the controllability of NW deposition, several alignment techniques have been introduced, including using parallel electrodes, rotating drums, switching electrodes, and biased rings.[32–39] These methods can control the overall alignment and orientation of NWs, but cannot precisely regulate location, alignment direction, and the number of individual NWs, so production of NW-based device array is still not feasible.

Electrohydrodynamic nanowire printing (e-nanowire printing) (Figure 1) enables accurate control of NW deposition; it freely adjusts the alignment, position, orientation, and the number of NWs.[40–61] e-nanowire printing provides a straight jet of polymer solution by keeping the nozzle tip within 1 cm of a grounded collector to preclude chaotic whipping of the liquid jet during its flight (Figure 2a).[40–61] A digitally controlled robotic stage aligns NWs line-by-line at the desired location on the substrate with high accuracy while moving in *x*- and *y*-directions.[40–61] Parallel stripes, perpendicular grids, and serpentine structures of wire can be printed by controlling movement of the stage. This ability to control individual NWs also facilitates fundamental study of confined 1D

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nanomaterials. Owing to many advantages of this additive NW printing with small material consumption, nanoelectronic devices based on large-scale-aligned NW arrays are being evaluated for use in energy harvesting, transistors, circuits, optoelectonics, memories, tissue engineering, and bioelectronics.[40–61] In this paper, recent development of highly aligned nanowires-based electronics is reviewed and research plans to achieve further progress in advanced nanoelectronics are suggested.

2. Semiconducting Nanowires for Electronic Devices

NWs can be made of solution-processed organic semiconductors (OSCs). Their chemical structures, conjugation system, crystallinity, and chain packing orientation affect charge transport properties of the wires, and can be easily modified.[1–9,26–28,44–46,51–54] Many electronic applications based on large-scale OSC NWs have been developed and show possibilities as next-generation electronic devices.[4–9,26–28,46,51–54] e-Nanowire printing has been used to produce highly aligned polymer NWs (Figure 2b), and to fabricate NW-based devices arrays over a large area.[51–54] Printed polymer NWs had circular cross section (Figure 2c).[51] Printing solutions were prepared by mixing OSCs with high-molecular-weight additive polymer (polyethylene oxide, PEO) (8:2, w:w), then OSC:PEO NWs were printed directly on the substrate.[51] The OSC and PEO phases separated into core (OSC) and shell (PEO) during the printing because the two polymers have different surface energies and solubility parameter difference in a solution with cosolvents system chlorobenzene and trichloroethylene.[51] Field-effect transistors (FETs) based on poly(3-hexylethiophene) (P3HT):PEO NWs and on poly{[*N*,*N*′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-*alt*-5,5′-(2,2′-bithiophene)} (N2200):PEO NWs showed typical p- and n-type field-effect charge transport characteristics with hole mobility μ_h = 0.015 $cm^2\ V^{-1}\ s^{-1}$ and electron mobility μ_e = 0.012 $cm^2\ V^{-1}\ s^{-1}$ (Figure 2d,e).[51] On-current of transistors was readily modulated by controlling the number of NWs; maximum on-current increased linearly with the number of wires.[51] Finally, an array of complementary inverters composed of p- and n-type NWs was fabricated; it showed switching gain of 17 and dynamic switching response.[51] This was the first demonstration of large-scale complementary inverter array with well-aligned OSC NWs. These results prove the feasibility of large-scale electronics arrays based on NWs.

Highly aligned OSC NWs were also used to demonstrate flexible and nonvolatile organic memory array on a ferroelectric dielectric layer (poly(vinylidene fluoride-*co*-trifluoroethylene), PVDF-TrFE).[52] The device showed quite different electrical characteristics before and after thermal annealing. In the pristine memory devices, unstable holes trapped by hydrophilic sites at the interface between the PEO shell and the PVDF-TrFE layer caused undesired release of H–F dipoles in PVDF-TrFE ferroelectric film; this release results in unstable threshold voltage and poor retention characteristics.[52] Thermal annealing of NWs (180 °C) induced dewetting of the PEO shell ($T_m \approx 65$ °C) and diffusion into P3HT core; as a result, the core–shell structure of P3HT:PEO NWs was transformed to molten PEO islands distributed on P3HT NWs.[52] Thermal annealing yielded a device with direct interface between P3HT and PVDF-TrFE layer and increased the retention time to $>10^4$ s and write/erase endurance cycles to >100 times.[52] The flexible OSC NW memory was also stable after 1000 mechanical bending cycles with radius of 5.8 mm.[52]

Recently, by mimicking memory properties of neurons and synapses in biological brain, artificial synaptic devices composed of ion-gel gate insulator and OSC NWs were developed (Figure 3a).[54] With gate voltage spikes which correspond to presynaptic spikes in biological

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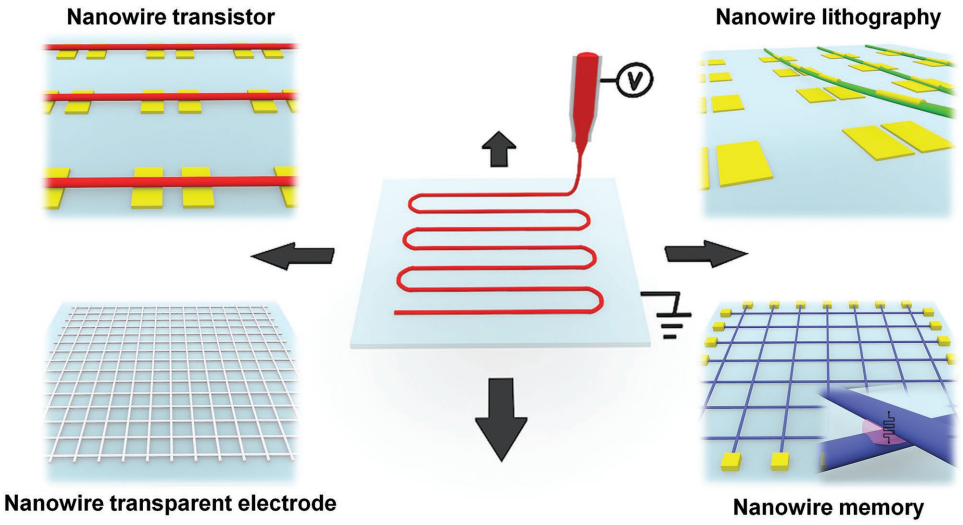

Figure 1. Various applications based on large-scale highly aligned nanowires array including nanowire transistor, nanowire transparent electrode, nanowire memory, and nanowire lithography.

synapse (Figure 3b), output current (postsynaptic current) was triggered (Figure 3c).[54] Single short-gate spike (–1 V, 50 ms) accumulated anions near OSC NWs, then holes were induced in the channel.[54] As a result, drain current was temporarily increased (Figure 3d).[54] After the spike, anion accumulation was released and drain current was returned to the initial current value, which is a similar response with short-term plasticity (STP) in biological synapse.[54] With repeated spikes of gate voltage (30 pulses, –1 V, 50 ms), accumulated anions diffused into the active channel and OSC NWs were electrochemically doped.[54] Resting current was longer than 5 min after the spikes, which is a similar response to long-term plasticity (LTP) (Figure 3e).[54] Energy consumption of NW synapse with channel length of 300 nm (≈1.23 fJ) was similar to that of biological synapse (≈10 fJ) and much lower than those of previous artificial synaptic devices (>1 pJ) owing to the large surface-to-volume ratio of ONWs and the short channel length of artificial synapse (Figure 3f).[54]

The semiconducting layer is the most important component in an electronic device. Therefore, these researches into preparation of highly aligned OSC NWs and demonstration of their electronic device applications suggest the great potential of NW-based future electronics.

3. Metal Nanowires for Transparent Nanoelectrodes

High-resolution patterning of electrodes on a sub-micrometer scale is an essential technology to fabricate high-density, transparent, flexible, and microminiature device arrays. In industry, photolithography and e-beam lithography are used to manufacture sub-micrometer electrodes, but these processes use expensive equipment, consume large amounts of materials, and are complicated. Compared to conventional printing methods such as drop-on-demand printing and transfer printing,[62–65] additive e-nanowire printing can improve electrode pattern resolution, processing speed, and efficient material consumption.[55–57]

Highly aligned and conductive metal NW arrays have been fabricated by printing composite NWs composed of high-molecular-weight binding polymer and metal precursors, then transforming the composite NWs to metal NWs by pyrolysis of binding polymer and metal precursors and concurrent nucleation and growth of metal nanoparticles (Figure 4a).[55] Polyvinylpyrrolidone (PVP)/silver trifluoroacetate (STA)/copper trifluoroacetate (CTA) composite NW arrays have been uniformly printed on the substrate and converted to silver nanowires (AgNWs) by calcining (350 °C).[55] Because the nanoscale Ag structure melts and agglomerates at relatively low temperature (200 °C),[16,17] a small amount of CTA was included in the composite NWs to form copper oxide (CuO) which has high melting temperature and maintains continuous structure of AgNW after calcining.[55] Large-scale-aligned AgNW arrays had an average diameter of 695 nm and low resistivity of 5.7 μΩ cm; which resulted in high transparency (94.7%), low sheet resistance (26.9 Ω $\square^{-1}$), and low optical haze (<1%) at wavelength of 550 nm.[55] Moreover, AgNW arrays showed good mechanical bending stability (>4000 times at bending radius of 7.5 mm) and thermal stability in air (up to 350 °C).[55]

FETs arrays that use two strands of AgNWs, one as 1D source and one as drain (S/D) nanoelectrode have been demonstrated.[55] All-NW FETs array with P3HT:PEO semiconducting NWs as active channels and nonionic

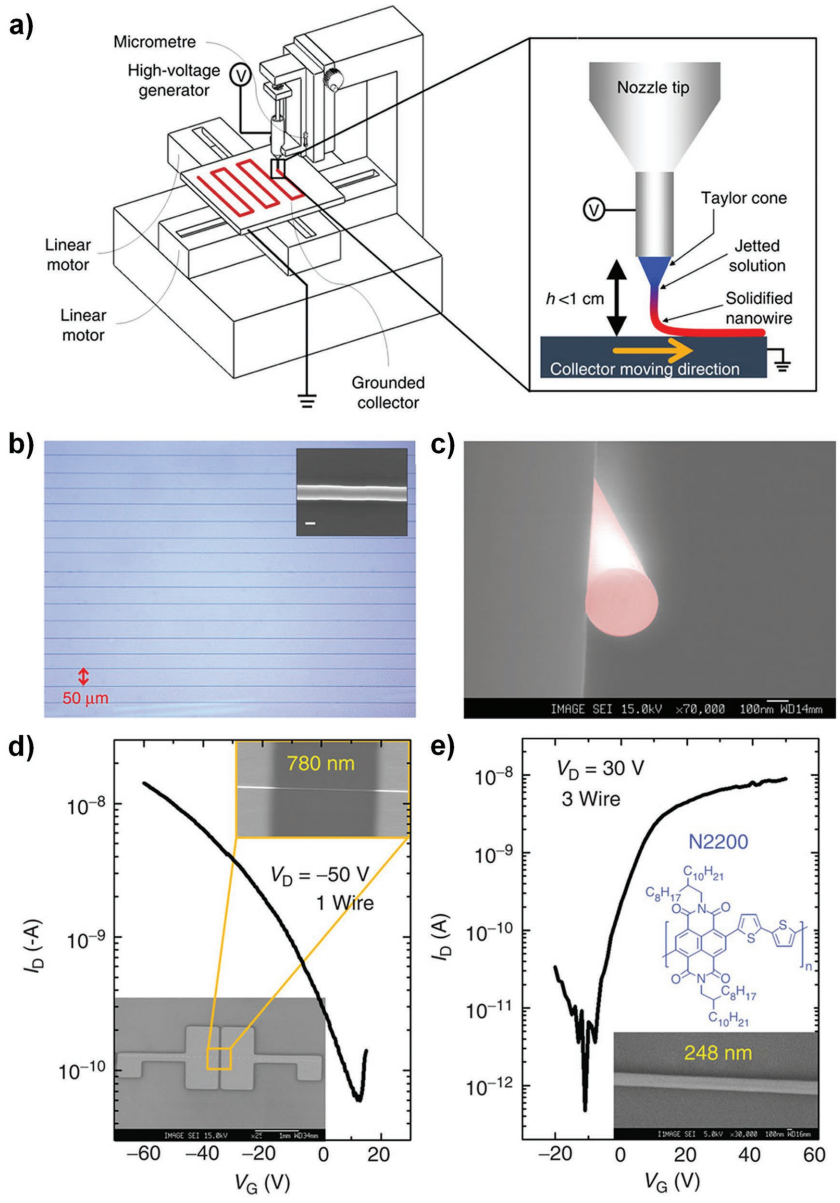

Figure 2. a) Schematic illustration of e-nanowire printing. b) Optical microscope image of highly aligned polymer NW arrays with 50 μm spacing. The diameter of NW is 290 nm (inset, scale bar, 200 nm). c) Scanning electron microscope image of cross section of a polymer NW. Reproduced with permission.[51] Copyright 2013, Nature Publishing Group.

PVDF-TrFE as a dielectric layer showed high field-effect mobility μ_h = 2.08 cm^2 V^{-1} s^{-1} (Figure 4b,c), because CuO with valence band edge (5.42 eV) on the surface of AgNWs increased the work function of electrodes to 5.1 eV, which closely matches the highest occupied molecular orbital of P3HT (5.2 eV).[55] Various channel lengths of FETs were readily fabricated by varying the spacing of AgNWs.[55] Drain current of pentacene thin film FETs decreased as channel length increased (Figure 4d).[55]

Indium zinc oxide (IZO) thin film FET arrays with AgNWs were also demonstrated.[55] AgNWs under the sputtered IZO film were thermally stable during a postannealing in air (250 °C, 1 h).[55] The device showed μ_e = 7.25 cm^2 V^{-1} s^{-1} that is lower than the previously reported μ_e of IZO transistor (≈20 cm^2 V^{-1} s^{-1}) because of the energy barrier between the work function of AgNWs (5.1 eV) and conduction band edge of IZO (3.45 eV).[55] However, compared with conventional a-Si TFT ($\mu \approx 1$ cm^2 V^{-1} s^{-1}), it is high enough to operate a commercial display.[55]

Organic light-emitting diodes, transparent heaters, and touch screen panels (TSPs) that exploit the high transmittance of highly aligned AgNW 2D electrodes, were also achieved (Figure 4e,f).[55] Maximum current efficiency of organic light-emitting diode (OLED) with AgNWs (100.1 cd A^{-1}) was higher than the control device with indium tin oxide electrodes (86.3 cd A^{-1}).[55] The transparent heater also showed uniform exothermic properties and the TSP operated stably without degradation.[55]

A polycrystalline copper nanowire (CuNW) array was produced using two steps of calcination.[56] The first step (500 °C, 1 h) in air transforms PVP/CTA composite nanowires to CuO NWs because Cu is easily oxidized in air.[56] To reduce CuO NWs to CuNWs, the second calcination was conducted in reducing gas (hydrogen) (300 °C, 1 h).[56] CuNW had a resistivity of 14.1 μΩ cm, which is slightly higher than that of bulk Cu (1.68 μΩ cm).[56] Interestingly, during the second calcination, Cu_xO at the junction of two crossed NWs did not reduce to Cu, but instead formed a CuNW-Cu_xO-CuNW sandwich structure (Figure 5a).[57] The existence of Cu_xO was confirmed by the elemental distribution analysis at the junction point of crossed NWs (Figure 5b–e).[57] This metal–oxide–metal (MOM) structure showed resistive switching properties. Compared to conventional deposition and lithographic methods for fabrication of MOM-structured memristors, e-nanowire printing is quite simple, inexpensive, and rapid. Crossbar-shaped CuNWs resistive memory had reliable nonvolatile memory operation with on/off current ratio of 10^6 and retention time > 2×10^4 s (Figure 5f,g).[57] Individually controlled and large-scale-printed metal NW electrode arrays would promote scaling down and high-density integration of electronics.

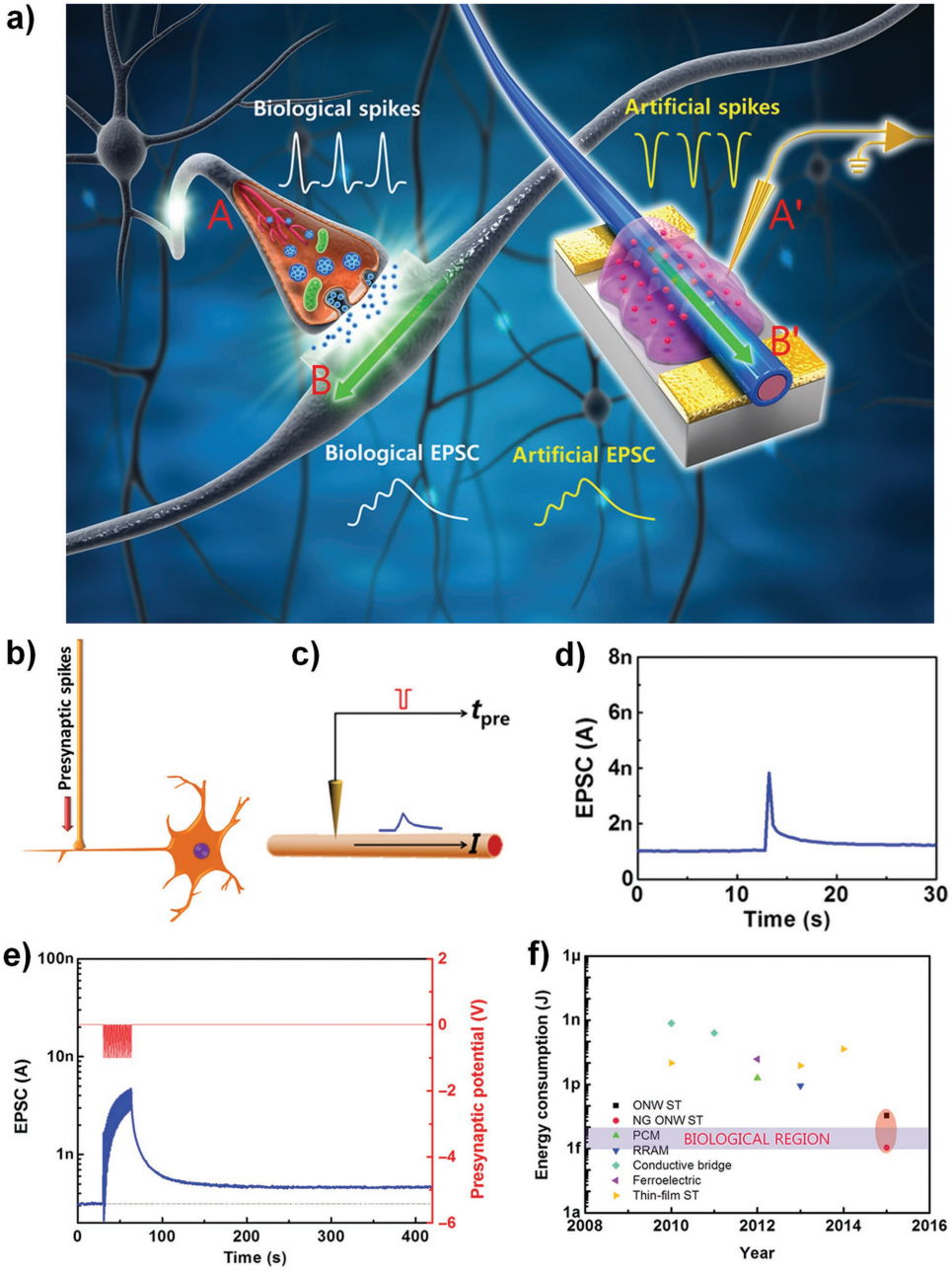

Figure 3. a) Schematic illustration of biological and artificial synapses. Schematic illustration of single presynaptic spike to b) a biological postneuron and c) an artificial OSC NW synapse. d) Excitatory postsynaptic current (EPSC) triggered by single presynaptic spike (–1 V, 50 ms). e) Postsynaptic current versus time of artificial OSC NW synapse triggered by 30 presynaptic spikes (–1 V, 50 ms); V_D (driving voltage) = 0.75 V. f) Energy consumption of artificial synaptic devices. NG, nanogap; PCM, phase change memory; RRAM, resistive switching random access memory. Reproduced with permission.[54] Copyright 2016, American Association for the Advancement of Science.

4. Polymer Nanowires for Nanowire Lithography

NW lithography can easily produce nanosized patterns or gaps by using polymer NW arrays as pattern masks.[58–61] To prepare the nanosized patterns reproducibly on a large area, a position-controllable mask NW is an essential requirement. Insulating polymer with low electrical conductivity is suitable for NW masks to exclude side effects or interactions of NW masks and other materials. Large-scale metal nanopatterns were simply fabricated using well-aligned insulating poly(9-vinyl carbazole) (PVK) NWs as a shadow mask for metal deposition.[51] Au thin layer deposited on PVK NWs was separated with a small gap of 350 nm after removal of the wire by sonication or exfoliation using adhesive tape.[51] The size of gaps is

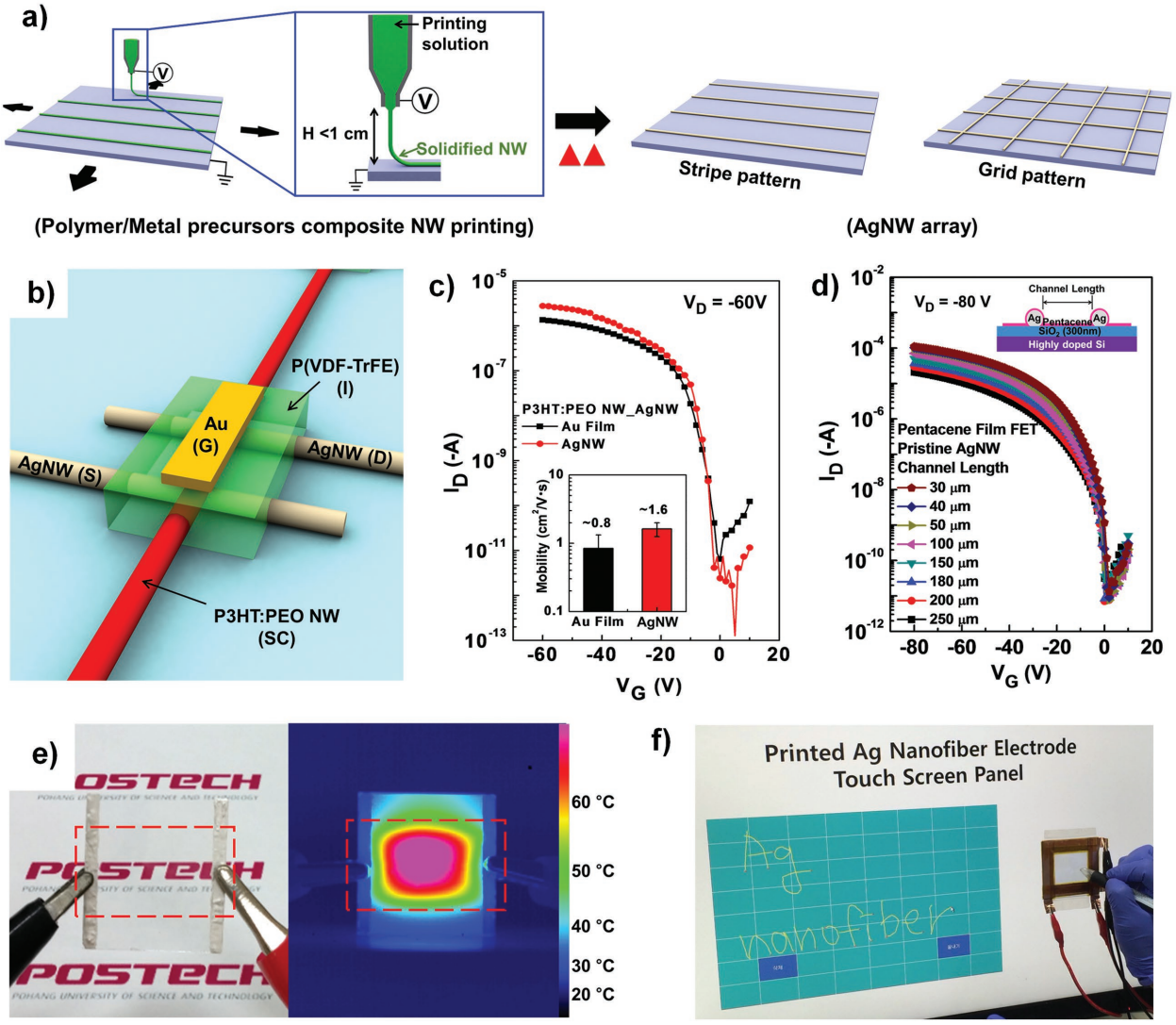

Figure 4. a) Schematic fabrication procedures of AgNW array. b) Schematic illustration of all-NW FETs with P3HT semiconducting NW, AgNW S/D nanoelectrodes, and P(VDF-TrFE) gate insulator. c) Transfer curves of all-NW FETs compared to P3HT NW FET with Au thin film electrodes (inset: comparison of mobilities between P3HT NW FET with Au film and AgNW S/D electrodes). d) Transfer curves of pentacene thin film FETs with the various channel length and AgNW S/D electrodes (inset: device structures). e) Digital and IR pictures of AgNW-based transparent heater with uniform heat distribution. f) Operation of AgNW array-based TSP by writing words "Ag nanofiber." Reproduced with permission.[55]

equivalent to the diameters of the mask wires, and therefore can be controlled easily.[51] Nanopatterned electrodes can be used to achieve transistors with short channel length which are essential for small, fast electronic applications. Short-channel P3HT:PEO (7:3, w:w) NW transistors with an ion-gel gate insulator were fabricated using Au film S/D electrodes with nanosized gap.[51] The short-channel devices showed very small contact resistance of 5.53 Ω cm and highest carrier mobility of 9.7 $cm^2\ V^{-1}\ s^{-1}$ (average 3.8 $cm^2\ V^{-1}\ s^{-1}$) with low drain voltage (–1 V) and gate voltage (–2 V).[51]

Printed NWs can also be used to prepare large-scale-aligned graphene nanoribbon (GNR) arrays by oxygen plasma etching of a graphene sheet, with PVK NWs as etching masks (Figure 6a).[58–60] Patterns of GNRs can be easily designed by printing patterns of PVK NWs (Figure 6b,c).[58] The narrowest GNR was 9 nm wide; the average was 16.05 ± 2.65 nm, which can be controlled by adjusting the diameter of wires and the etching time.[58] Raman spectrum of GNRs showed a D peak at 1350 cm^{-1} caused by irregular edge disorders and oxidized dangling bonds in the GNR, which are absent in defect-free pristine graphene sheets.[58]

Using patterned GNR, transistor with channel length of 50 μm had μ_h = 300 $cm^2\ V^{-1}\ s^{-1}$ and on/off current ratio of 70 (Figure 6d). Moreover, 144 GNR transistor arrays

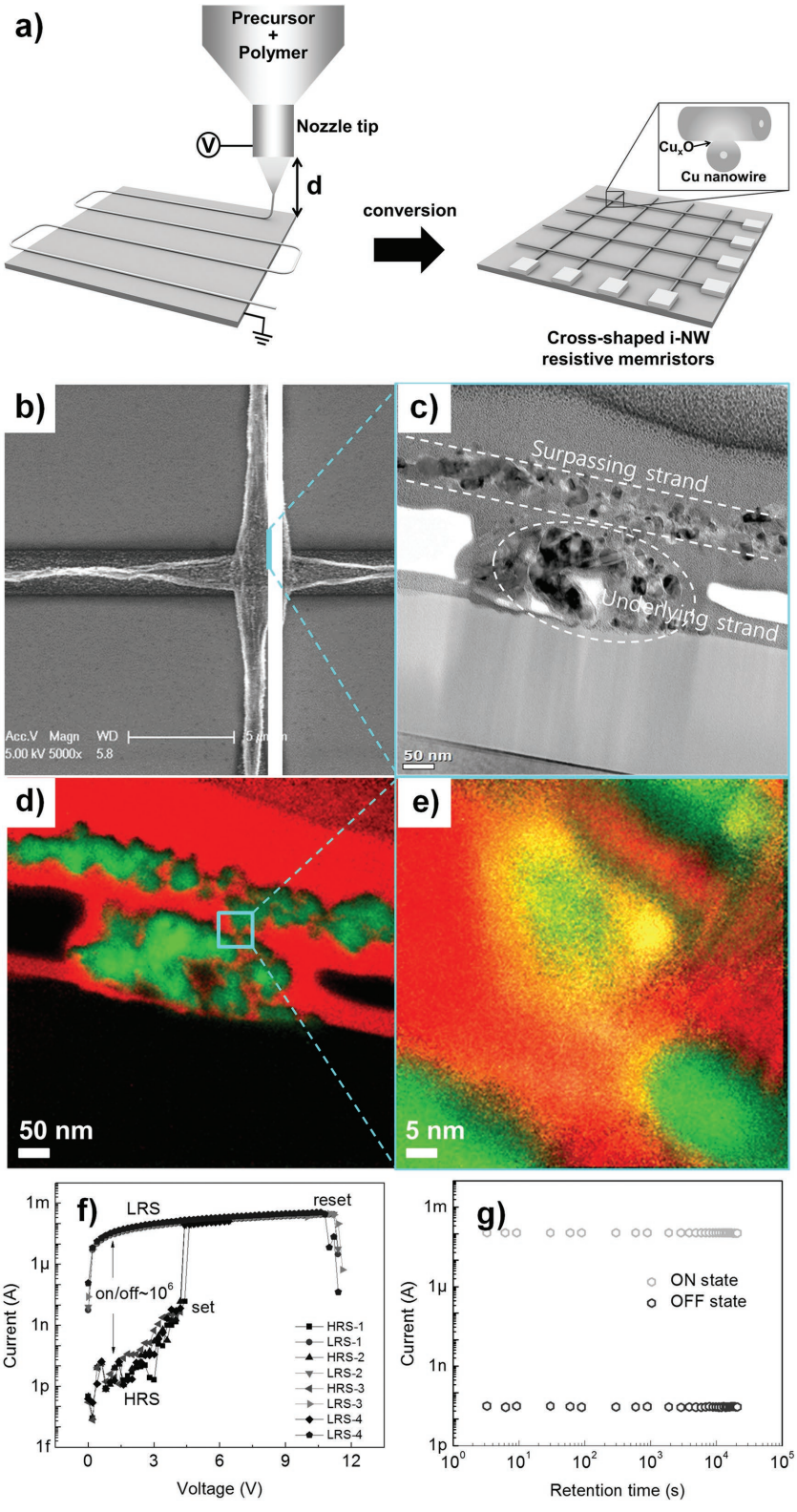

Figure 5. a) Schematic fabrication process of cross-shaped CuNW memristors. b) Scanning electron microscope images of two perpendicular CuNWs focused on intersection for focused-ion-beam cut. c) Transmission electron microscope image of cross section of two crossed wires, and d) relative elemental mapping by electron energy loss spectroscopy (green: Cu; red: C; yellow: O), and e) magnified elemental mapping of the connecting part of two crossed wires. f) Current–voltage plot of the resistive switching behavior of a cross-shaped CuNW resistive memristor. g) Retention of ON/OFF states of the memristor. Reproduced with permission.[57]

were readily fabricated on the 4 in. wafer.[58] Geometry selection (armchair/zigzag) and edge quality control of patterned GNRs are still challenging, but these results demonstrate a promising strategy to develop graphene-based future electronics.

Printed NW mask was also used as very narrow separators between pixels in OLEDs (Figure 7a).[61] PVK NW separate thin Al layer effectively, and can replace conventional pixel-isolation procedures, which are expensive and complicated (Figure 7b).[61] On the anode, 1 μm thick insulating PVK wires were printed, then thin organic layers and cathode were deposited (total thickness <100 nm) (Figure 7c).[61] Wire separators separated the OLED pixels and minimized loss of light emission area due to shading by separators.[61] Therefore, almost the same current efficiency, luminance, and current density were achieved from green OLEDs with or without 40 PVK wires.[61] Large-area (3 cm × 3 cm) white OLEDs with two PVK wires were demonstrated and divided into three 3 cm × 1 cm subpixels (Figure 7d).[61] Each subpixel was operated selectively. A large-area (3 cm × 3 cm) flexible matrix-type OLED with 5 × 5 pixels with PVK wires was also successfully demonstrated and showed the potential for use in future lighting and display products (Figure 7e).[61]

5. Conclusions

NW printing techniques to achieve large-scale and individually controllable alignment are very promising because they facilitate development of nanoelectronic devices in an easier, cheaper, faster, and more efficient way compared

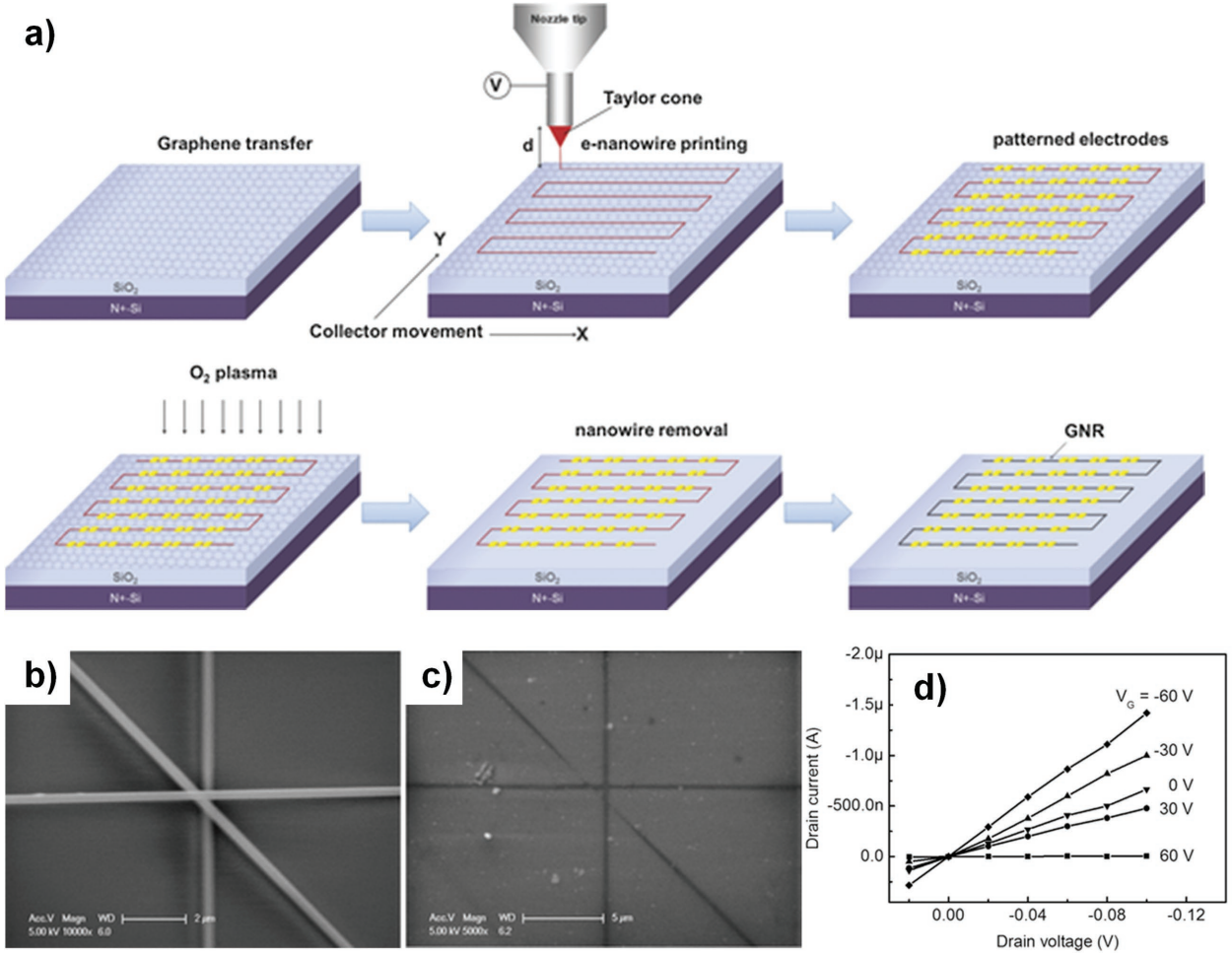

Figure 6. a) Schematic fabrication process of large-scale GNRFET array. Scanning electron microscope images of b) PVK NWs and c) GNRs aligned in star pattern. d) Output curves of GNRFETs. Reproduced with permission.[58]

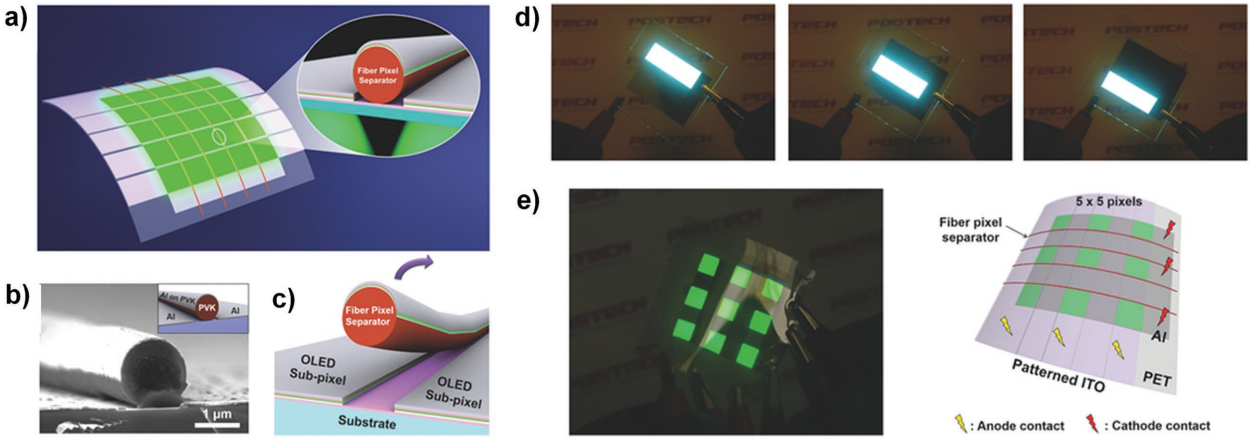

Figure 7. a) Schematic image of fiber pixel separators in OLEDs. b) Scanning electron microscope image of cross section of Al film (40 nm) deposited PVK wires (inset: schematic image). c) Schematic illustration of the mechanism of pixel separation based on nanowire lithography. d) Digital images 3 cm × 3 cm large-area white OLED with three 3 cm × 1 cm subpixels patterned by PVK wire pixel separators. e) Digital image and schematic illustration of flexible matrix-type OLED with 25 pixels patterned by PVK wire pixel separators. Reproduced with permission.[61]

to conventional nanoscale device fabrication methods. Various large-scale electronic applications based on unique properties of 1D nanomaterials have been fabricated using organic and inorganic NW arrays; examples include transistors, memories, optoelectronic devices, and energy harvesters. Additive printing of NWs has flexibility to freely customize patterns of NWs on 2D plates, and can produce 3D structures by stacking NWs, so that high-density-integrated devices that transcend Moore's law might be achieved using aligned NWs in the future. To widen the field of NW-based electronics, diverse materials should be developed in the form of NWs, and fundamental research into their morphological, electrical, and optical properties of 1D nanomaterials should be performed to enhance understanding of them. Furthermore, industrial-scale manufacture of NW-based electronics would be accompanied by development of equipment, processing, and materials; progress in this field is essential to realization of future advanced electronics.

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